REMARKS

Present Status of Application

The Examiner is thanked for his continued indication that claims 3-7, 10-14, and 17-20 are allowable. The Office Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 102(e) as allegedly unpatentable over U.S. Patent 6,499,129 B1 to Srinivasan et al. Applicant respectfully traverses the rejections and requests reconsideration and withdrawal of all rejected claims.

Summary

The present application is directed to a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program, which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise-level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and

uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Applicant respectfully traverses the rejections and submits that they should be withdrawn for separate and independent reasons. As more fully detailed below, Srinavasan is not prior art to the present application (or at least has not been properly supported as prior art), since the present application predates the filing date of Srinavasan. Further, and more significantly, there are significant substantive distinctions between the Applicant's claimed invention and Srinavasan, as applied by the Office Action.

Srinivasan is NOT Prior Art to Applicant's Invention

Srinivasan is not prior art to the invention of the present application, and all rejections base on Srinivasan should be removed for at least this reason. The filing date of Srinivasan is July 21, 1999. The filing date of the present application is March 22, 1999, which predates the filing date of Srinivasan. Accordingly, the rejections under 35 U.S.C. § 102(e) are misplaced, inappropriate, and should be withdrawn.

Applicant acknowledges that Srinivasan claims the priority benefit of a provisional application that was filed on July 22, 1998. However, this priority benefit ONLY applies to the extent that materials of the Srinivasan patent are disclosed in the provisional application. In this regard, 35 U.S.C. § 102(e) states:

> A person shall be entitled to a patent unless ... the invention was described in a patent granted ***on an application for patent by another filed in the United States*** before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title [35 USC §371(c)(1), (2), (4)] before the invention thereof by the applicant for patent, ...

As is clear from 35 U.S.C. § 102(e), the filing date of an application is not automatically treated as the filing date of a provisional application to which priority is claimed. To properly support the alleged rejection, the Examiner must provide a copy of the provisional application and an identification as to where (in the provisional application) the cited subject matter is disclosed (since it is the Examiner's burden to form a *prima facie* rejection).

Notwithstanding the foregoing, and to advance the prosecution of this application, Applicant hereby advises the Examiner that the present invention was both conceived and reduced to practice prior to the filing date of the provisional application to which Srinavasan claims priority. The Applicant has not submitted a 131 declaration to accompany this response, as such is not believed to be necessary based in part upon the substantive distinction set out below, and in part upon the misplaced reliance upon (and application of) Srinavasan, as noted above. Should, however, the Examiner maintain his reliance upon Srinavasan, and mail a subsequent Office Action that provides a copy of the provisional application (with the requisite support for a proper rejection), then Applicant may respond with a 131 declaration at that time. It is noted, however, that any such ensuing Office Action should be made non-Final, as it will set forth new grounds of rejection that are not necessitated by any amendment.

For at least the foregoing reasons, Applicant respectfully requests that the rejection be withdrawn and all claims passed to issuance.

Substantive Distinctions of the Srinivasan Patent

Turning now to the specific rejections, the Office Action rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 102(e), as being anticipated by Srinivasan et al. Applicant respectfully traverses this rejection for at least the reasons that follow.

Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

Likewise, claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of independent claims 1 and 15 for at least the reason that Srinivasan fails to disclose or teach at least the features emphasized above.

Srinivasan is directed to a system and method for estimating ***performance*** of integrated circuit designs. Significantly, the Office Action does not even specifically allege that Srinivasan teaches the features emphasized above. Instead, the Office Action only

generally alleges that Srinivasan anticipates the claimed invention, insofar as Srinivasan is directed to a

> ... method and system for estimating design performances, including cross-coupling effects, simultaneous switching, etc. with feature limitations identical to the claims (Summary of the Invention, col. 5, lines 18-32)... The design rule checker is to check transistor susceptible to noise in the cross-talk influence (col. 5, lines 18-32, for example), including checking noise susceptible or noise immunity in the deep submicron of the transistor circuit design (Summary of the Invention).

(Office Action, paragraph spanning pages 2 and 3).

Applicant respectfully submits that this rejection embodies fundamental misapplications of the teachings of Srinivasan. First, the undersigned performed an electronic search of the entire text of the specification and claims of the Srinivasan patent, which search confirmed that the term "noise" is not used anywhere in the claims or specification of Srinivasan. Therefore, the allegation by the Office Action that Srinivasan teaches a system or method to check for the susceptibility of ***noise*** immunity is simply and clearly misplaced. For this reason alone, the rejection set forth in the Office Action is fundamentally misplaced and should be withdrawn.

Further, and as a separate and independent basis for the patentability of claims 1 and 15, claim 1 specifies the ***analysis of widths of field effect transistors within a static gate***, to determine whether the gate has an acceptable ***noise immunity*** (claim 15 includes similar features). Simply stated, Srinivasan does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. The undersigned performed an electronic search of the entire text of the Srinivasan patent for the individual terms "noise," "transistor," and "width." As noted above, the term "noise" is not used or mentioned anywhere in either the specification or claims of the Srinivasan patent. With regard to the terms "transistor" and

"width," the only relevant mention of these terms in the Srinivasan patent is at col. 5, line 48 through col. 6, line 20, which states:

> In step 308, a layout for the integrated circuit is created. The layout can be manually generated or automatically generated. The layout is typically contained in a database file such as a GDSII format file. The layout contains polygons and geometries on various layers that are used to generate the mask set for fabricating the integrated circuit. In step 312, parasitic and other parameters affecting circuit performance are extracted from the layout. Before the layout is prepared, the design engineer cannot be certain of what the parasitic capacitance and resistance the nets will be. ***Using the layout, the lengths, widths, area, and sizes of various circuit paths are measured.*** The capacitance and resistance parameters for a process technology are defined in a technology model file. Using these process parameters and the circuit path information, the parasitic capacitances and resistances are calculated. Parasitic capacitance and resistance creates propagation delays based on resistance-capacitance (RC) delay.
>
> ...
>
> Although the techniques may be applied with any, process technology, in an embodiment, the invention specifically handles CMOS technology. CMOS technology makes use of PMOS and NMOS transistors. A MOS transistor has drain, gate, source, and substrate or well connections. ***A size of a MOS transistor is defined by its gate width (W) and channel length (L).*** The principles of the invention are applicable to designs using technologies other than MOS transistor technology by analogy. For example, an NMOS transistor has a source and a drain which are analogous to the collector and emitter of a npn bipolar transistor.

As can be confirmed from even a cursory review of the foregoing, the cited portion of Srinivasan does not teach the features emphasized above in claims 1 and 15. More significantly, there is absolutely no mention or reference anywhere in Srinivasan as to the analysis of FET widths to determine whether or not a particular gate has a shortfall with respect to ANY design concern (much less whether the gate has an acceptable level of noise immunity, as required by independent claims 1 and 15).

Consequently, and for at least this separate and independent reason, independent claims 1 and 15 patently define over Srinivasan, and the rejections based on Srinivasan should be withdrawn.

Further, the Office Action repeatedly cites col. 5, lines 18-32 if Srinivasan as allegedly teaching a number of aspects of the claimed invention. It does not. In fact, this cited location of Srinivasan states only:

> A system including a computer or other programmed machine executing electronic design automation (EDA) software is used in the design of integrated circuits. EDA software tools include schematic editors, performance estimation software, circuit simulators, layout editors, design rule checkers, parasitic extractors, and many others. In a preferred embodiment, the techniques of the present invention are implemented in an EDA software program and executed on a computer. The software of the present invention provides performance estimation and verification of integrated circuits. The software may be stored on a mass storage device such as a disk drive or other computer readable medium, and then loaded (partially or entirely) into the memory of the computer for execution.

As can be verified from even a cursory review of this cited portion of Srinivasan, there is absolutely no teaching of significant features embodied in both independent claims 1 and 15, including: "evaluation of a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity." For at least these additional, and fundamental, shortcomings of Srinivasan, the rejections of independent claims 1 and 15 should be withdrawn.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claims 1 and 15 is misplaced and should be withdrawn. For at least these same reasons, claims 2 and 16, which depend from claims 1 and 15, respectively, patently define over Srinivasan as well.

Claims 8 and 9

The Office Action also rejected claims 8 and 9 under 35 U.S.C. § 102(e), as being anticipated by Srinivasan. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Srinivasan fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8, relying on the same portions of Srinivasan that the Office Action relied upon in rejecting claim 1. In this regard, the Office Action relied principally upon col. 5, lines 18-32 (quoted above) and secondarily upon col. 6, lines 10-41 (also partially quoted above). Simply stated, and for the same reasons discussed in connection with claims 1 and 15 above, Srinivasan does NOT teach at least the features of claim 8 that are emphasized above (i.e., "evaluating a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity."

Consequently, and for the same reasons set forth in connection with claim 1, Applicant respectfully submits that the rejection of claims 8 is misplaced and should be withdrawn. For

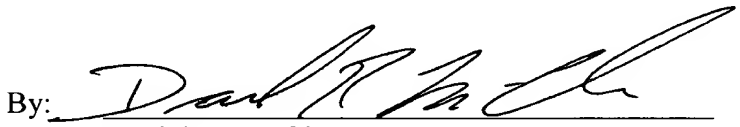
at least these same reasons, claim 9, which depends from claim 8, patently defines over Srinivasan as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

By: 

Daniel R. McClure
Registration No. 38,962

770-933-9500